

Customer No.: 31561  
Application No.: 10/707,870  
Docket No.: 12049-US-PA

### AMENDMENTS

Please amend the application as indicated hereafter.

1. (currently amended) An electrostatic discharge (ESD) protection circuit coupled to a first pad of an integrated circuit, the integrated circuit having a plurality of system voltage sets, the system voltages including a first system voltage and a first ground voltage, the ESD protection circuit comprising:

a first common conductive line;

a first diode, a cathode of the first diode coupled to the first common conductive line, an anode of the first diode coupled to the first system voltage;

a first P-type transistor, a first S/D terminal and a gate terminal of the first P-type transistor coupled to the first system voltage, a second S/D terminal of the first P-type transistor coupled to the first pad; and

a first N-type transistor, a first S/D terminal of the first N-type transistor directly coupled to the first common conductive line, a gate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first pad.

2. (original) The ESD protection circuit of claim 1, further comprising a second N-type transistor, a first S/D terminal of the second N-type transistor coupled to the first pad, a gate terminal and a second S/D terminal of the second N-type transistor coupled to the first ground voltage.

3. (original) The ESD protection circuit of claim 2, further comprising:

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a second common conductive line;  
a second diode, an anode of the second diode coupled to the first ground voltage, a cathode of the second diode coupled to the second common conductive line; and  
a third diode, an anode of the third diode coupled to the second common conductive line, a cathode of the third diode coupled to the first ground voltage.

4. (currently amended) The ESD protection circuit of claim 1, wherein the ESD protection circuit is coupled to a second pad of the integrated circuit, the plurality of system voltage sets further comprises a second system voltage and a second ground voltage, and the ESD protection circuit further comprises:

a fourth diode, a cathode of the fourth diode coupled to the first common conductive line, an anode of the fourth diode coupled to the second system voltage;

a second P-type transistor, a first S/D terminal and a gate terminal of the second P-type transistor coupled to the second system voltage, a second S/D terminal of the second P-type transistor coupled to the second pad; and

a third N-type transistor, a first S/D terminal of the third N-type transistor coupled to the first common conductive line, a gate terminal of the third N-type transistor coupled to the second ground voltage, a second S/D terminal of the third N-type transistor coupled to the second pad.

5. (original) The ESD protection circuit of claim 4, further comprising a fourth N-type transistor, a first S/D terminal of the fourth N-type transistor coupled to the second pad, a gate terminal and a second S/D terminal of the fourth N-type transistor coupled to the second ground voltage.

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6. (original) The ESD protection circuit of claim 5, further comprising:

a second common conductive line;

a fifth diode, an anode of the fifth diode coupled to the second ground voltage, a cathode of the fifth diode coupled to the second common conductive line; and

a sixth diode, an anode of the sixth diode coupled to the second common conductive line, a cathode of the sixth diode coupled to the second ground voltage.

7. (original) An electrostatic discharge (ESD) protection circuit coupled to a first pad of an integrated circuit, the integrated circuit having a plurality of system voltage sets, the system voltages including a first ground voltage, the ESD protection circuit comprising:

a first common conductive line;

a first diode, a cathode of the first diode coupled to the first ground voltage, an anode of the first diode coupled to the first common conductive line; and

a first N-type transistor, a first S/D terminal of the first N-type transistor coupled to the first pad, a gate terminal and a substrate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first common conductive line.

8. (original) The ESD protection circuit of claim 7, wherein the plurality of voltage systems further comprises a first system voltage, and the ESD protection circuit further comprises:

a second common conductive line;

a second diode, a cathode of the second diode coupled to the second common conductive line, an anode of the second diode coupled to the first system voltage;

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a first P-type transistor, a first S/D terminal and a gate terminal of the first P-type transistor coupled to the first system voltage, a second S/D terminal of the first P-type transistor coupled to the first pad; and

a second N-type transistor, a first S/D terminal of the second N-type transistor coupled to the second common conductive line, a gate terminal of the second N-type transistor coupled to the first ground voltage, a second S/D terminal of the second N-type transistor coupled to the first pad.

9. (original) The ESD protection circuit of claim 7, wherein the ESD protection circuit is coupled to a second pad of the integrated circuit, the plurality of system voltage sets further comprises a second ground voltage, and the ESD protection circuit further comprises:

a third diode, a cathode of the third diode coupled to the second ground voltage, an anode of the third diode coupled to the first common conductive line; and

a third N-type transistor, a first S/D terminal of the third N-type transistor coupled to the second pad, a gate terminal and a substrate terminal of the third N-type transistor coupled to the second ground voltage, a second S/D terminal of the third N-type transistor coupled to the first common conductive line.

10. (original) The ESD protection circuit of claim 9, wherein the system voltages further comprises a second system voltage, and the ESD protection circuit further comprises:

a second common conductive line;

a fourth diode, a cathode of the fourth diode coupled to the second common conductive line, an anode of the fourth diode coupled to the second system voltage;

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a second P-type transistor, a first S/D terminal and a gate terminal of the second P-type transistor coupled to the second system voltage, a second S/D terminal of the second P-type transistor coupled to the second pad; and

a fourth N-type transistor, a first S/D terminal of the fourth N-type transistor coupled to the second common conductive line, a gate terminal of the fourth N-type transistor coupled to the second ground voltage, a second S/D terminal of the fourth N-type transistor coupled to the second pad.

11. (currently amended) An electrostatic discharge (ESD) protection circuit coupled to a pad of an integrated circuit, the integrated circuit having a system voltage and a ground voltage, the ESD protection circuit comprising:

a P-type transistor, a first S/D terminal and a gate terminal of the P-type transistor coupled to the system voltage, a second S/D terminal of the P-type transistor coupled to the pad;

a first N-type transistor, a first S/D terminal of the first N-type transistor directly coupled to the system voltage, a gate terminal of the first N-type transistor coupled to the ground voltage, a second S/D terminal of the first N-type transistor coupled to the pad; and

a second N-type transistor, a first S/D terminal of the second N-type transistor coupled to the pad, a gate terminal and a second S/D terminal of the second N-type transistor coupled to the ground voltage.

12. (new) The ESD protection circuit of claim 11, further comprising a diode, a cathode of the diode coupled to a common conductive line, an anode of the diode coupled to the system voltage.